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EXAMINER	
NGUYEN, HIEP	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,124	VAN WERSHOVEN, LOESJE MARIA JACOBA	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a) because they fail to show **an output driver** as described in the specification. In the specification, page 2, element 4 is described as the standard inverter. Figure 1 of the present application shows that circuit 4 **is not an output driver**. Circuit 4 comprises two **identical** transistors connected in cascode having gates coupled together. When a voltage is input to the gates, both transistors are turned on at the same time. Thus, circuit 4 functions as a switch, a variable resistor or a voltage divider. Moreover, element 4 does not have an **input terminal** thus, it is not a driver that is designed to "drive" an input signal.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: the disclosure "An output driver such as the **standard inverter** reference 4" in figure 1, page 2 is misleading. Element 4 in figure 1 comprises two transistors of the **same type (N-channel)**, they will be turned on or off at the same time when a voltage is applied to the gates.

Therefore, **element 4 cannot be a standard inverter**. The disclosures "a core region 2", a periphery region 3", "contacts Vddq5 and Vssq6" are misleading because in figure 1, **any point** of the schematic of figure 1 could be defined as a "a core region 2", "a periphery region 3", "contacts Vddq5 and Vssq6". The applicant is requested to make a **clear definition** what are the "a core region 2", "a periphery region 3", "contacts Vddq5 and Vssq6" in this circuit. The disclosure " The output driver is constructed **without substrate contacts** which has the result that **a capacitor** 10 is present between the Vssd contact 7 and the Vssq contact 6" " is misleading because any element or circuit which is **build on a substrate** must be contacted with that substrate unless that circuit is build in the open air close to the substrate. It is also not clear how a **capacitor** can be present when the output driver is constructed **without substrate contacts.** The disclosure "The output driver 4 may either be slew- rate controlled or not slew-rate controlled" is misleading because the "output driver is not a driver (standard inverter) and there is no possibility that the "output driver" is slew-rate controlled. As disclosed, element 4 is an "output driver" then this "output driver" cannot function as a driver because there is **no input terminal for receiving the input signal**. Two **identical** transistors connected in cascode as shown in figure 1 cannot be a driver (such as a standard inverter) because these transistors are of the same type. They will be turned on at the same time when a signal is applied to the input (not shown).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1-3 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In claim 1, the recitation

"An integrated circuit provided with at least one output driver **without contacts to a substrate** and further provided with at least a core region with a Vssc contact, and a periphery region provided with at least one Vssq contact" is non enable. The "output driver" recited is not a driver because there is **no input terminal for receiving the input** signal. Two **identical** transistors connected in cascode having gates coupled together. When a voltage is input to the gates, both transistors are turned on at the same time. Thus, circuit 4 is not a driver and the circuit of figure 1 is not an integrated circuit that function as an output driver. The recitation " **without contacts** to a substrate" is non-enable because it is impossible to fabricate an IC circuit on a substrate without having any contact between the circuit and the substrate.

Regarding claims 2 and 3, the recitation "an output driver" has the same 112, 1st paragraph mentioned above.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "An IC circuit....to a substrate" is indefinite because it is misdescriptive. Figure 1 of the present application shows that circuit 4 **is not an output driver**. Circuit 4 comprises two **identical** transistors connected in cascode having gates coupled together. When a voltage is input to the gates, both transistors are turned on at the same time. Circuit 4 functions as a switch, a variable resistor or a voltage divider. The recitation "**without contacts** to a substrate" is indefinite because it is misdescriptive. In the integrated circuit fabrication, the circuit is fabricated on the substrate through different processes: photolitography, diffusion, ion implantation, metallization, etc. Therefore, it is misdescriptive to recite "at least one output driver **without contacts to a substrate**". It is not clear what the "a core region" and the "a periphery region" are meant by. The specification fails to define what they are. Figure 1 of the present application is only a **schematic** of an

integrated circuit without having clear support or indication proving what the "a core region" and the "a periphery region" are. The specification discloses that 2 is "a core region" and 3 is "a peripheral region". Figure 1 shows that "2" and "3" are merely **two spots located above a supply line** on the schematic. Thus, **any spot** on the schematic can be defined as "a core region" and " a peripheral region". The same analysis is true for the recitations "a Vssc contact" and "a Vssq contact". They can be **any spot** on the circuit that have a certain voltage because in the Remarks, the Applicant admitted that " the Vssc contact and the Vssq contact these contacts can be located **anywhere** along the nodes shown in FIG 1" (page 5, lines 14-16). **The Applicant is requested to explain clearly** what are the "a core region", " a peripheral region", "a Vssc contact" and "a Vssq contact". The Applicant is requested to explain how element 4 can be **a driver circuit**. The specification is misleading when it discloses that circuit 4 is "a standard inverter" (page 2, lines 21-22).

Regarding claims 2 and 3, the recitation " output driver" is indefinite because it is misdescriptive. With the structure of the circuit 4, it can only be a switch, a variable resistor or a voltage divider.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by So (US Pat. 6,028,465).

Regarding claim 1, figure 4 of So shows an integrated circuit provided with at least one output driver (23) "without contacts to a substrate" and further provided with at least a core region (2) with a Vssc contact (A), and a periphery region (3) provided with at least one Vssq contact (B), characterized in that a resistance (R1) with a value lying between 100 and 300 ohms (col. 4, lines 27-33) is provided between each Vssq contact and the Vssc contact. Note that figure 4 of So shows no contacts to the substrate.

are

Claims 1 and 3, ~~is~~ rejected under 35 U.S.C.102 (b) as being anticipated by Asprey et al. (US Pat. 5,193,200).

Regarding claim 1, figure 3 of Asprey shows an IC circuit having an output driver (314) "without substrate contacts" having a resistance (312) provided between a "Vssc contact" (A) in a "core region" (2) and a "Vssq contact" (B) in a "periphery region" (3). This resistance has a value of 100 Ohms (col. 9, lines 30-33).

Regarding claim 3, output driver (314) is slew-rate controlled and resistor (312) has a value (100 Ohms) smaller than 250 Ohms. Note that the resistor and the capacitor (304) at the output of the driver (314) control the slew rate of the output signal. Note that figure 3 of Asprey shows no contacts to the substrate.

are

Claims 1 and 2, ~~is~~ rejected under 35 U.S.C.102 (e) as being anticipated by Bridgewater, Jr. (US Pat. 6,307,401).

Regarding claim 1, figure 4 of Bridgewater shows an IC circuit having an output driver (104) "without substrate contacts" having a resistance (122) provided between a "Vssc contact" (A) in a "core region" (2) and a "Vssq contact" (B) in a " periphery region" (3). This resistance has a value of 100-300 Ohms (col. 7, lines 14-15).

Regarding claim 2, output driver (104) is not slew-rate controlled and resistor (122) has a value (300 Ohms) greater than 250 Ohms. Note that figure 4 of Bridgewater shows no contacts to the substrate.

are

Claims 1 and 2, ~~is~~ rejected under 35 U.S.C.102 (e) as being anticipated by Schell et al. (US Pat. 6,642,768).

Regarding claim 1, figure 4 of Schell shows an IC circuit having an output driver (not shown connected to output (Vref) "without substrate contacts" having a resistance (R2b) provided between a "Vssc contact" (A) in a "core region" (2) and a "Vssq contact" (B) in a " periphery region" (3). This resistance has a value of 300 Ohms (col. 7, lines 35-36).

Regarding claim 2, output driver not slew-rate controlled and resistor (R2b) has a value (300 Ohms) greater than 250 Ohms. Note that figure 4 of Schell shows no contacts to the substrate.

Response to Arguments

In the Remark, page 4, the Applicant fails to explain what are the "core region" and the "peripheral region". Showing misleading disclosure in the specification is not enough to solve indefiniteness of the claims. The specification simply discloses: "Fig. 1 shows a circuit 1 with a core region 2 and a periphery region 3 in a simplified diagrammatic form". As understood by the examiner, the "core region 2" and the "peripheral region 3" (shown above the supply line of the circuit) can be **any spots** that locate in different parts of the schematic. For the same reason discussed above, the "Vssq contact" and the "Vssc contact" can be any spot in the schematic that have potentials as confirmed in the Remarks: the **"**exact location" of the "Vssc contact" and the "Vssq contact," these contacts **can be located anywhere along the nodes shown in FIG. 1"**.

In page 5 of the Remarks, the Applicant fails to explain what " without substrate contact". The explanation: "the **phrase without substrate contacts**, as known to one of ordinary skill in the art, this **refers to the lack of contacts to the substrate of the integrated circuit** is not adequate enough. The Applicant fails to explain why an integrated circuit built on a substrate does not have any contact with the substrate. As known to one of ordinary skill in the art, to built a circuit on a substrate, the following fabrication steps have to be followed: photolitography, diffusion, ion implantation, metallization etc. Thus, there is no point to state that an integrated circuit has no contacts to the substrate. In conclusion, any circuit of the prior art of record used for art rejection has "core region", peripheral region", "Vssc contact" and "Vssq contact".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

02-07-04

TUAN T. LAM
PRIMARY EXAMINER